(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
31 January 2002 (31.01.2002)

PCT

(10) International Publication Number
WO 02/09179 A1

(51) International Patent Classification[7]: H01L 23/31

(21) International Application Number: PCT/EP01/07841

(22) International Filing Date: 6 July 2001 (06.07.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0018028.1 24 July 2000 (24.07.2000) GB

(71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventor: CUTTER, John, R.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agent: STEVENS, Brian, T.; Internationaal Octrooibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

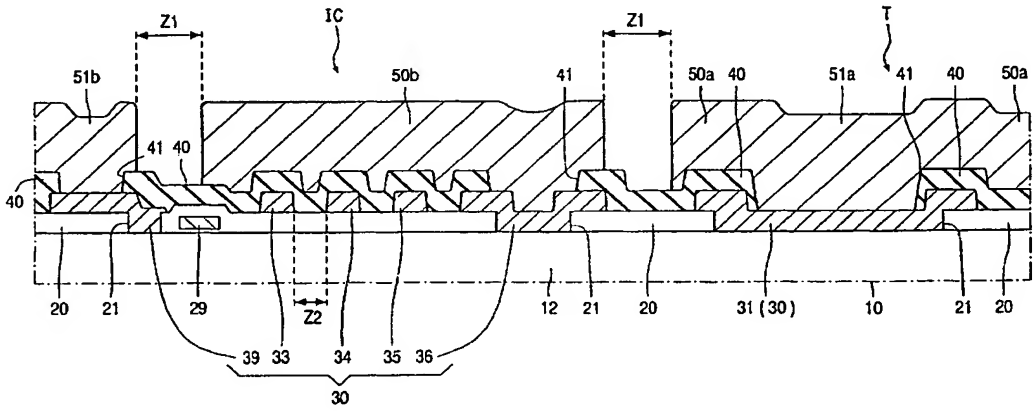
(81) Designated State *(national)*: JP.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: RESIN SEALED SEMICONDUCTOR DEVICE WITH STRESS-REDUCING LAYER



(57) Abstract: Thermal cycling can lead to damaging stress at the upper surface of a semiconductor device chip (10) encapsulated in synthetic resin material (100), particularly in the case of power devices that include an IC. The invention provides a thick ductile layer pattern (50) of, for example, aluminium over most of the top surface of the insulating over-layer (40) of the chip (10). Electrically-isolated parts (50a, 50b, 50c, 50d etc.) of this ductile covering are individually connected to respective underlying conductive areas so as to reduce charging effects across the insulating over-layer (40). A sufficient spacing Z1 is present between these isolated parts (50a, 50b, 50c, 50d etc.) to avoid short circuits as a result of deformation by shearing and smearing during thermal cycling of the device. The ductile metal layer pattern (50) reduces stress between the insulating material (40) and the plastic material (100), but it can be both easily and cheaply applied in device manufacture before dividing the wafer into individual chips.

WO 02/09179 A1